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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RIYAMI, ABDULLA A	

ART UNIT	PAPER NUMBER
2616	

NOTIFICATION DATE	DELIVERY MODE
11/28/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/772,737	BASSO ET AL.	
	Examiner	Art Unit	
	Abdullah Riyami	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02 May 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date: _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because in figure 1, block 34, "DCB" should be –FCB—and in figure 2, it is suggested to change "Indivudal Flow" to –Individual Flow--. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly labeled as "Annotated Sheets" and must be presented in the

amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d)(1). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

Claim Objections

3. Claims 3,14, 15, and 22 are objected to because of the following informalities:

As per claim 3, line 3, it is suggested to remove "hierarchy control block" since it is a repetition in line 2.

As per claim 14, line 4, it is suggested to remove "calendar control blocks" since it is a repetition from line 3.

As per claim 15, line 3, it is suggested to change "control blocks" to –the control blocks--.

As per claim 22, line 5, it is suggested to change "the block content" to –block content--.

Claims 16, 23 and 24 are objected sine they depend on claims 15 and 22.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-8 and10-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lakshmanamurthy et al. (US 2004/0004964) in view of Elmaliach et al. (US 6922732).

As per claim 1, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1) comprising: a plurality of SRAM and DRAM memory devices external to the scheduler (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35); Control blocks of

scheduling elements stored in said memory devices with at least some of the memory devices storing more than one type of control block (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35) wherein

a) SRAM memory is used if the content of a control block is Read-Modify-Write at packet enqueue and at dequeue (see paragraph 14, 17, 41, 43, 52, and 55);

b)SRAM and DRAM memory are used if the control block content is Read-Modify-Write only, at the packet dequeue (see paragraph 14,17, 41, 43, 47,51, 52, and 55); and

c)DRAM memory is used if the control block content is Read only at packet enqueue and dequeue (see paragraph 14,17, 19, 33, and 47).

Lakshmanamurthy et al. does not expressly disclose a hierarchical structure.

Elmaliach et al. discloses a hierarchical structure (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical structure (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

As per claim 2, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1), wherein DRAM memory is preferentially used if the Read-Modify-Write content is only at the packet dequeue (see paragraph 14, 17, 41, 43, 47, 51, 52, and 55).

As per claim 3, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1), wherein the control blocks include flow queue control blocks, frame control flow blocks, hierarchy control blocks, target port queue control blocks, hierarchy control blocks and schedule control blocks (see paragraphs 11 and 12).

As per claim 4 and 5, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1), a physical port bandwidth which is divided into a plurality of logical links (see paragraph 40 and figure 4), the bandwidth available to each of the logical links is divided into a plurality of VLANs (see paragraphs 40 and 26 can be implemented in VLAN). And also wherein physical port bandwidth resources for non-hierarchical links are shared among individual traffic flows (see paragraphs 12, 40 and 26).

Lakshmanamurthy et al. does not expressly disclose hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows.

Elmaliach et al. discloses hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical pipeline arrangement for link resource sharing serving multiple queues (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

As per claim 6, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1), wherein memory access to enqueue tasks does not conflict with memory access allocated to dequeue tasks (see paragraph 13).

As per claim 7, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1), wherein a first SRAM contains a set of data buses and stores flow queue control blocks that are required for 'read' and 'write' at each flow queue enqueue and dequeue time, and a second SRAM containing two data buses, one dedicated to 'read' and one dedicated to 'write', and stores frame control blocks and VLAN hierarchy control blocks (see figure 1, block4 140, 124, 122, 112, 114, 119, 127, 130, figure 4, see paragraphs 12 and 55).

As per claim 8, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1), wherein a first DRAM stores a network management counter and a second DRAM stores flow queue control blocks and VLAN hierarchy control blocks that require 'read' only at both enqueue time and dequeue time

(see figure 1, block4 140, 124, 122, 112, 114, 119, 127, 130, figure 4, see paragraphs 12, 13, 19, and 55).

As per claim 10 and 11, Lakshmanamurthy et al. discloses a method for retrieving and pipelining information for a network traffic scheduler (see figure 1), a physical port bandwidth which is divided into a plurality of logical links (see paragraph 40 and figure 4), the bandwidth available to each of the logical links is divided into a plurality of VLANs (see paragraphs 40 and 26 can be implemented in VLAN). And also wherein physical port bandwidth resources for non-hierarchical links are shared among individual traffic flows (see paragraphs 40 and 26).

Lakshmanamurthy et al. does not expressly disclose hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows.

Elmaliach et al. discloses hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical pipeline arrangement for link resource sharing serving multiple queues (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

As per claim 12, Lakshmanamurthy et al. discloses a structure for a hardware scheduler pipeline (see figure 1) comprising a plurality of control blocks (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35); a plurality of memory devices external to the scheduler in which the control blocks are stored (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35), at least some of the memory devices sharing more than one type of control block (see paragraph 12).

Lakshmanamurthy et al. does not expressly disclose a hierarchical pipeline arrangement for link resource sharing serving multiple queues.

Elmaliach et al. discloses a hierarchical pipeline arrangement for link resource sharing serving multiple queues (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical pipeline arrangement for link resource sharing serving multiple queues (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

As per claim 13, wherein the hierarchical pipeline arrangement sharing serves the multiple queues within an approximated fixed period of time (see paragraph 19).

As per claim 14, the control blocks include, from the group consisting of flow queue control blocks, frame control blocks, calendar control blocks, target port queue control blocks, calendar control blocks and hierarchy control blocks (see paragraphs 11 and 12).

As per claim 15, the control blocks that are accessed less frequently within a fixed period of time are stored in DRAM memories, and control blocks that are accessed with higher frequency within a fixed period of time are stored in SRAM (see paragraph 12).

As per claim 16, basic flow QCB is stored in SRAM memory (see paragraph 14, 17, 41, 43, 52, and 55) and dequeue/enqueue read only flow QCB is stored in DRAM memory (see paragraph 14, 17, 19, 33, and 47).

As per claim 17, Lakshmanamurthy et al. discloses a method for retrieving and pipelining information for a network traffic scheduler (see figure 1), a physical port bandwidth which is divided into a plurality of logical links (see paragraph 40 and figure 4), the bandwidth available to each of the logical links is divided into a plurality of VLANs (see paragraphs 40 and 26 can be implemented in VLAN).

Lakshmanamurthy et al. does not expressly disclose hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows.

Elmaliach et al. discloses hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical pipeline arrangement for link resource sharing serving multiple queues (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

As per claim 18, time-based calendar arrays for guaranteed bandwidth service and weighted fair queueing calendar arrays for allocation of available bandwidth for competing flows at each port when no service is required by the time-based calendars (see figure 1, well known that scheduler program may use weighted round robin scheduling algorithm or any other type of scheduling algorithm).

As per claim 19, each of the calendar arrays contains three pointers comprising a current position pointer, a current time pointer and a next position pointer each of the calendar arrays (see paragraph 55).

As per claim 20, the time-based calendar provides a scheduling function for flow queues and VLANs (see paragraphs 40 and 26 can be implemented in VLAN).

As per claim 21, the weighted fair queueing calendar provides best effort scheduling in flow queues, VLANs and logical links (see figure 1, well known that scheduler program may use weighted round robin scheduling algorithm or any other type of scheduling algorithm).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 9 and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Lakshmanamurthy et al. (US 2004/0004964).

As per claim 9, Lakshmanamurthy et al. discloses a method for retrieving and pipelining information for a network traffic scheduler (see figure 1), wherein the information is stored in a plurality of SRAM and DRAM devices comprising storing functional queue control blocks in the SRAM and DRAM devices (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35), wherein control block content that is Read-Modify-Write at both packet enqueue and dequeue time is stored in SRAM devices (see paragraph 14, 17, 41, 43, 52, and 55); control block content that is Read-Modify- Write packet only at dequeue time is stored in either SRAM or DRAM devices (see paragraph 14,17, 41, 43, 47,51, 52, and 55); and control block content that is read only either at enqueue or dequeue time is stored in DRAM devices (see paragraph 14,17, 19, 33, and 47).

As per claim 22, Lakshmanamurthy et al. discloses an article of manufacture comprising a computer usable medium having a computer readable program embodied

in the medium, wherein the computer readable program, when executed on a computer (see paragraph 60), causes the scheduler to store functional queue control blocks in external memory storage devices comprising a mix of SRAM and DRAM devices based on the block content at enqueue and dequeue time (see paragraphs 11-15 and 55), and to share the external devices among the control blocks (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35).

As per claim 23, Lakshmanamurthy et al. discloses an article of manufacture, wherein the program causes a control block content having Read-Modify-Write at both enqueue and dequeue time to be stored in SRAM (see paragraph 14, 17, 41, 43, 52, and 55); a control block content having Read-Modify-Write at only dequeue time to be stored in either SRAM or DRAM (see paragraph 14,17, 41, 43, 47,51, 52, and 55); and a control block content having 'read' only to be stored in DRAM (see paragraph 14,17, 19, 33, and 47).

As per claim 24, Lakshmanamurthy et al. discloses an article of manufacture, wherein the program causes the scheduler to select a flow queue to egress for each duration of a scheduler tick using a time-based calendar or a weighted fair queuing calendar (see figure 1, well known that scheduler program may use weighted round robin scheduling algorithm or any other type of scheduling algorithm).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdullah Riyami whose telephone number is (571) 270-3119. The examiner can normally be reached on Monday through Thursday 8am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on (571) 272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AR

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